REMARKS

The Office Action dated January 11, 2005, has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1, 2, 7, 8, 12, 13, 22-24, 28, 31, 32, 41-43, 51, 52, 56 and 57 have been amended to more particularly point out and distinctly claim the subject matter of the invention. No new matter is added, and no additional search and/or consideration is required. Thus, claims 1-60 are presently pending in the subject application and are respectfully submitted for consideration.

Claims 1-60 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,021,132 (*Muller et al.*) in view of U.S. Patent No. 6,529,519 (*Steiner et al.*) The Office Action took the position that *Muller* disclosed all the elements of the claimed invention, with the exception of "a single buffer for packet mechanism." *Steiner* was cited as curing the deficiencies in *Muller*, and the Office Action alleged that it would have been obvious to a person of ordinary skill in the art to combine *Muller* and *Steiner* to achieve the claimed invention. Applicants respectfully submit that the cited references, either alone or in combination, do not disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 2-7 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address

Resolution Table. The memory structure also includes a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 8, upon which claims 9-12 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table having an associative memory structure and using a key to index a location within the Address Resolution Table. The Address Resolution Table resolves addresses in a packet-based network switch. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 13, upon which claims 14-27 are dependent, recites a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table. The memory structure also includes a Transmit Descriptor Table. The Transmit Descriptor Table is associated with a corresponding packet-based

network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The memory structure also includes a Packet Storage Table. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 28, upon which claims 29-31 are dependent, recites a packet-based switch. The packet-based switch includes a shared memory structure having an Address Resolution Table and a Packet Storage Table. The packet-based switch also includes a key to index a location within the Address Resolution Table. The packet-based switch also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 32, upon which claims 33-51 are dependent, recites features including the patentable features of claim 13, but is drawn to a packet-based switch.

Claim 52, upon which claims 53-56 are dependent, recites features including the patentable features of claim 8, but is drawn to a packet-based switch.

Claim 57, upon which claims 58-60 are dependent, recites features including the patentable features of claim 8, but is drawn to a packet-based switch.

As discussed in the specification, examples of the present invention enable a memory structure to resolve addresses in a packet-based network switch. The present invention enables bandwidth savings that are attributed to a one buffer-per-packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated. Thus, a packet-based switch performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. Overhead is reduced and a reduction in accesses per frame is achieved. The single access for both read and write can be attributed to the single-entry direct-mapped address table. It is respectfully submitted that the cited references of *Muller* and *Steiner*, when viewed alone or combined, fail to disclose or suggest all the elements of the presently pending claims. Therefore, the cited references fail to provide the critical and unobvious advantages discussed above.

As discussed in the previous response, *Muller* relates to shared memory management in a switch network element. *Muller* describes a shared memory manager 220 to provide a level of indirection that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer pointers are preallocated during

the initialization of switching element 100 and requested from shared memory manager 220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without having to duplicate the packet data.

Steiner relates to prioritized-buffer management for fixed size packets in a multimedia application. *Steiner* describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. *Steiner* also describes a shadow register for storing conflict-free updates from the tag register and a page register for storing pointers to the lowest free or unoccupied page. *Steiner* also describes a buffer that is organized along packet boundaries or pages for convenience of operation. A processor, or MPU 34, maintains a table of pointers to each packet boundary, and, therefore, knows the location of all leftover packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22.

Applicants submit that *Muller* and *Steiner*, either alone or in combination, do not disclose or suggest "an Address Resolution Table . . . using a key to index a location within the Address Resolution Table" and "a single buffer per packet mechanism . . . for enabling an execution of a single access in order to locate an entire packet at the location using the key," as recited in claim 1. Applicants also submit that independent claims 8, 13, 28, 32, 52 and 57 recite the patentable features of claim 1. Thus, applicants submit

that the cited references do not disclose or suggest at least these features of the pending claims.

Applicants submit that the cited references, either alone or in combination, do not disclose or suggest using a key to index a location in an address table. Referring to *Muller*, pointers are allocated to buffers as packets are received at the input port. As noted above, the buffers are kept on hand to allow storage of received data packets. The pointers of *Muller*, however, do not disclose or suggest a key to index a location in the Address Resolution Table. Further, *Muller* describes a data packet being stored in more than one buffer. Thus, *Muller* does not disclose or suggest enabling an execution of a single access in order to locate an entire packet at the location using the key. Applicants submit that *Muller* does not disclose or suggest locating an entire packet using a key, but uses the stored pointers to piece together a packet which may be stored over several buffers. Thus, *Muller* does not disclose or suggest at least these features of the pending claims.

Applicants also submit that *Steiner*, either alone or in combination with *Muller*, does not disclose or suggest all the features of the pending claims. *Steiner* describes using pointers and a tag register to each packet boundary within a buffer, also known as "pages." *Steiner*, however, does not disclose or suggest using a key to index a location within the buffer, or to a page within the buffer. Instead, *Steiner* uses a processor to maintain a table of pointers and the tag register. The processor does not use a key to index the table of pointers or the tag register. Further, the processor reads the contents of

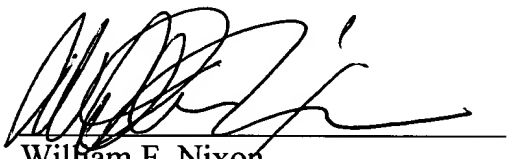
a shadow register to determine how many packets are in a buffer. Thus, *Steiner* does not disclose or suggest a single buffer per packet mechanism for enabling an execution of a single access in to locate an entire packet at the location using the key. For at least these reasons, applicants submit that the cited references, either alone or in combination, do not disclose or suggest at least these features of claims 1-60. Applicants respectfully request that the obviousness rejection be withdrawn.

It is further submitted that each of claims 1-60 recites subject matter that is neither disclosed nor suggested by the cited references. It is therefore respectfully requested that all of claims 1-60 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



William F. Nixon
Registration No. 44,262

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802
WFN:noe/cct